

10/21/60  
09/00584  
JCS-72 U.S. PTD

Class	Subclass	ISSUE CLASSIFICATION

## U.S. UTILITY Patent Application

<p><b>O.I.P.E.</b></p> <p>SCANNED <u>5852</u> Q.A. <u>UO</u></p>	<p><b>PATENT DATE</b></p>
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APPLICATION NO.	CONT/PRIOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
09/805841	F	205	10T	1322	Leagle / Nicolan
<p>Toshiki Inoue Kyoko Kumagai</p> <p>204 242 1742</p>					
<p>Electrolytic plating method and device for a wiring board</p>					

<b>ISSUING CLASSIFICATION</b>									
<b>ORIGINAL</b>			<b>CROSS REFERENCE(S)</b>						
<b>CLASS</b>	<b>SUBCLASS</b>		<b>CLASS</b>	<b>SUBCLASS (ONE SUBCLASS PER BLOCK)</b>					
<b>INTERNATIONAL CLASSIFICATION</b>									

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	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.				<b>NOTICE OF ALLOWANCE MAILED</b>	
	(Assistant Examiner)	(Date)			
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____  _____				<b>ISSUE FEE</b>	
	(Primary Examiner)	(Date)		Amount Due	Date Paid
<input type="checkbox"/> The terminal ____ months of this patent have been disclaimed.				<b>ISSUE BATCH NUMBER</b>	
	(Legal Instruments Examiner)	(Date)			
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